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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,584	03/29/2004	Heng-Chih Lin	TI-36611	2093

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EXAMINER	
CHOW, CHARLES CHIANG	
ART UNIT	**PAPER NUMBER**
2618	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,584	LIN ET AL.	
	Examiner	Art Unit	
	Charles Chow	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8,10-14,18 and 20* is/are rejected.

7)☒ Claim(s) *5-7,9,15-17 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Objection

1. Claim 4 is objected to because of the following informalities:

In line 1 of claim 4, the informality, "(FIG.2A)", needs to be removed. Appropriate correction is required.

It is suggested the word "Claim" in the first line of each dependent claims, to be changed to "claim".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 8, 10-11, 14, 18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over See (US 2004/0005,869 A1) in view of Pickering et al. (US 6,242,965 B1).

For claim 1, See teaches a circuit [harmonic rejection mixer 11 in Fig. 1 & Fig. 5] for providing a reduced harmonic content output signal that is modulated according to an input signal [the I, Q, input signal to 11 to modulate the local oscillator signals derived from 4XLO in Fig. 5; the removing of the unwanted harmonics from the output of 11 based upon the multiple clock phases & the weighted current source in paragraph 0040], the circuit comprising

a harmonic rejection mixer [11 in Fig. 5, paragraph 0039-0042] configured to use the input signal [I, Q inputs to mixer Gilbert cells 85-90 in Fig. 5] to modulate a combination of the oscillator output signals [to modulate the oscillator signals from 81 to 84 of the divider 23 in Fig. 4], the oscillator output signals being respectively weighted so as to provide an

emulated sinusoidal signal constituting the reduced harmonic content output signal [the oscillator signals from 81-82 are respectively weighted in Gilbert cells 86 & 89 with the scaled current source of square root of 2 , paragraph 0040, to provide desired harmonic rejection, which is equivalent to applicant's weighted legs in paragraph 0076-80].

See fails to teach further features in this claim.

Pickering teaches an oscillator circuit [circuit in Fig. 16] including at least one circuit portion configured to receive first and second orthogonal oscillator input signals [REF1, REF2] having respective first and second phases [the phase regeneration 162_1 to 162n in Fig. 16, each receives two oscillator signals, REF1 & REF2, in quadratue, orthogonal, having respective phase offset to each other in col. 1, lines 58-62], and

to provide plural oscillator output signals having respective mutually distinct phases that are interpolated between the first and second phases [to produce phase shifted oscillator outputs DRCLK1 to DRCLKn, each with distinct predetermined phase offset in abstract & col. 2, lines 4-10, such as from reference clocks in Fig. 3a; phase interpolation 222 in Fig. 8 to interpolate the references CLK1, CLK2], in order to provide the carrier signal to be modulated in a communication device [col. 1, lines 27-35]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade See with Pickering's plurality of oscillator signals with different phase offset from phase interpolation 222, control current 226, in order to provide the carrier signal to be modulated in a communication device.

For claims 4, 10, 14, 20, See teaches the harmonic rejection mixing circuit in Fig. 5, but fails to teach other features in this claim.

Pickering teaches the wherein at least one of the circuit portions includes at two phase interpolation circuits [the two circuit for 91a/b & 92a/b of the phase interpolation 222 in Fig. 9], each phase interpolation circuit being configured to provide a respective one of the oscillator output signals, by combining at least two weighted oscillator input signals; or by, performing, weighted summing of currents of respectively representing at two oscillator input signals [the output DRCLK is provided by summing the weighted current derived from CLK1, CLK1-bar, CLK2, CLK2-bar at 91a/b & 92a/b, which is controlled by the weighted current sources I1+, I1-, I2+, I2-, derived from current source circuitry 226 with control PS [1-6] in Fig. 10; col.],

using the same reason in claim 1 above, to combine Pickering's teaching to See.

For claims 8, 18. See teaches the harmonic rejection mixing circuit in Fig. 5, but fails to teach other features in this claim. Pickering teaches the wherein: the oscillator output signals are equally spaced in phase [the equally spaced sum phase in the table in col. 10, lines 1-34; the phase angle is determined by weighted currents & W1, W2 in col. 8, lines 19-24].

For claim 11, See teaches a method [the harmonic rejection mixer 11, in Fig. 1 & Fig. 5, paragraph 0039-0045] for providing a reduced harmonic content output signal that is modulated according to an input signal [the I, Q, input signal to 11 to modulate the local oscillator signals derived from 4XLO in Fig. 5; the removing of unwanted harmonics from the output of 11 based upon the multiple clock phases & the weighted current source in paragraph 0040], the method comprising

using the input signal [I, Q inputs to mixer Gilbert cells 85-90 in Fig. 5] to modulate a combination of the oscillator output signals [to modulate the oscillator signals from 81 to 84, from the divide by 4 counter 23 in Fig. 4], respectively weighted so as to provide an

emulated sinusoidal signal constituting the reduced harmonic content output signal [the oscillator signals from 81-82 are respectively weighted in Gilbert cells 86 & 89 with the scaled current source of square root of 2 , paragraph 0040, to provide desired harmonic rejection, which is equivalent to applicant's weighted legs in paragraph 0076-80].

See fails to teach further features in this claim.

Pickering teaches the receiving first and second orthogonal oscillator input signals having respective first and second phases [the phase regeneration 162_1 to 162n in Fig. 16, each receives two oscillator signals, REF1 & REF2, in quadratue, orthogonal, having respective phase offset to each other in col. 1, lines 58-62];

providing plural oscillator output signals having respective mutually distinct phases that are interpolated between the first and second phases [to produce phase shifted oscillator outputs DRCLK1 to DRCLKn, each with distinct predetermined phase offset in abstract & col. 2, lines 4-10, such as from reference clocks in Fig. 3a; phase interpolation 222 in Fig. 8 to interpolate the references CLK1, CLK2], in order to provide the carrier signal to be modulated in a communication device [col. 1, lines 27-35]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade See with Pickering's plurality of oscillator signals with different phase offset from phase interpolation 222, control current 226, in order to provide the carrier signal to be modulated in a communication device.

3. Claims 2-3, 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over See in view of Pickering, as applied to claims 1, 11 above, and further in view of Chen (US 6,359,486 B1).

For claims 2, 12, See teaches the harmonic rejection circuit in Fig. 5. See & Pickering fail to teach further features in these claims.

Chen teaches the oscillator circuit [Fig. 7] is configured to provide the oscillator output signals [OUT & OUTB] in response to only a first pair of orthogonal oscillator input signals [Φ0, Φ1 in Fig. 7, Fig. 8] and a second pair of orthogonal oscillator input signals [Φ0B, Φ1B] that are opposite in phase to the first pair of orthogonal oscillator input signals [Fig. 8 shows the waveform that Φ0B, Φ1B are opposite phase from Φ0, Φ1 respectively], in order to generate a better phase shifted oscillator signal by utilizing the high speed, higher frequency, low power, phase interpolation [col. 1, lies 5-10]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade See & Pickering with Chen high speed, low power, phase interpolation, in order to generate a better oscillator signal.

For claims 3, 13, See teaches the harmonic rejection circuit in Fig. 5, but fails to teach further features in these claims.

Pickering teaches the oscillator input signals are of a same frequency as the oscillator output signals [[first & second reference signals are of common frequency & set to the same frequency as it's output frequency in col. 2, lines 42-46], and are not derived from a frequency-division of higher frequency oscillator input signals [the output is derived from the mixing the quadrature input signals, col. 2, lines 4-10], using the same reason in claim 1 above for combining Pickering's teaching to See & Chen.

Claims Objection

4. Claims 5-7, 9, 15-17, 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

For claim 5, 15, the prior arts fail to teach the exactly four circuit portions to receive the different combinations of I, I-, Q, Q-, signals. **For claim 6, 16**, the prior arts fail to teach the four circuit portions, to provide the respective eight oscillator output signals with phase interpolated between different combinations of I, I-, Q, Q-, signals, based on claims 5, 15. **For claim 7, 17**, the prior arts fail to teach the four circuit portions, to provide respective ninth to twelfth outputs, having phase substantially matching respective one of the I, or I-, or Q or Q-, input signal, based on claims 6, 16. **For claim 9, 19,** the prior arts fail to teach an array of load equalization buffers, configured to weight the oscillator output in accordance with the strength of the legs, how much contribution from each leg, for the reducing of the harmonic output signal.

The cited prior arts in the following are considered: **See, Pickering, Chen, Yang (US 2005/0175,132 A1), Lee et al. (Us 6,512,408 B2), Donnelly et al. (US 5,808,498), Routh et al. (US 3,296,517), Kuwano (US 6,359,523 B1), Martin te al. (US 2003/0016,762 A1), Malone et al. (US 2005/0032,486 A1), Persico (US 5,574,755), Kimppa et al. (US 6,373,345 B1), Beards et al. (US 6,417,712 B1).**

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. **(US 6,359,523 B1), Kuwano** teaches the orthogonal modulator in Fig. 2, abstract, having the 90 degree phase shifter 5 for output 4 oscillator signal to I/Q mixer 3, for frequency up conversion.

B. **(US 2005,0032,486 A1), Malone et al.** teach the LO phase interleaver 326 and the polyphase circuit 321 for producing four local oscillator signals 322-325 [paragraph 0040].

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Chow whose telephone number is (571) 272-7889. The examiner can normally be reached on 8:00am-5:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Chow CC.

June 8, 2006.

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